NED UNIVERSITY
OF ENGINEERING AND TECHNOLOGY

Course/Course Code:

Data Acquisition and Microcontroller (MC-546)

Lecture # 06

Course Teacher:

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Bus Basics

- ☐ A bus is a set of physical wires and connectors that carries digital information between two or more systems or between two or more parts of a system in a specified format.
- ☐ A bus allows two or more devices to communicate with each other, generally for the purpose of transmitting data. A bus can be either internal or external to a system.
- ☐ A sending device can also be a receiving device, and a receiving device can also be a sending device. Figure 1 illustrates the concept of a typical bus.

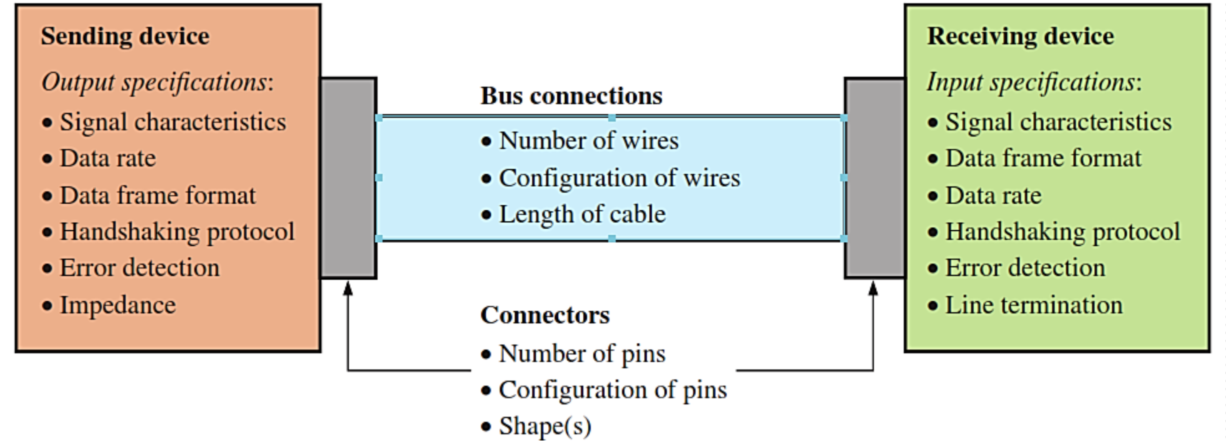


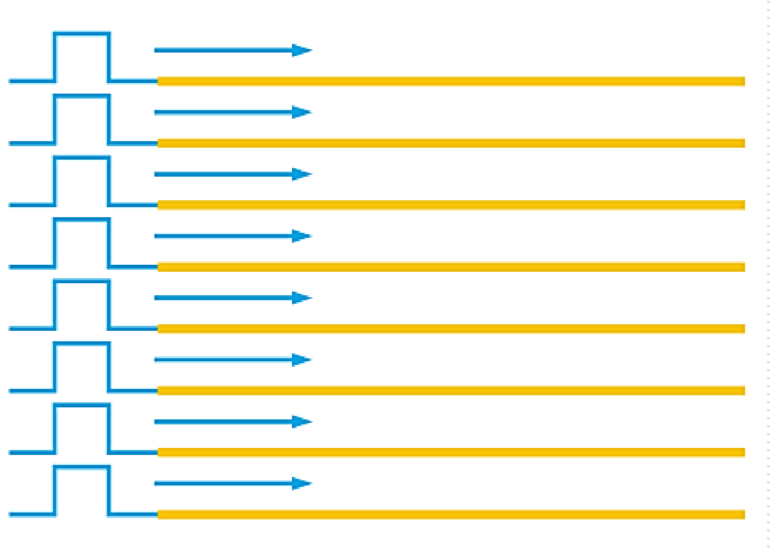
Figure: Physical and electrical definition of a typical bus

Properties of Bus

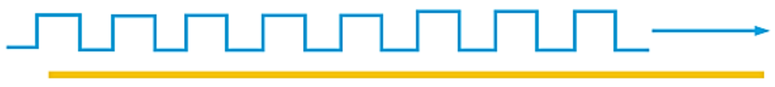
- Each device connected to a bus must be compatible with the bus specifications in order to communicate.
- The **physical properties** of a typical bus include the number of wires or PCB conductors (width), the configuration and length of the wires or conductors, and the types and configurations of the connectors.
- The **electrical properties** of a typical bus include but are not limited to some or all of the following: signal format, signal voltage levels, clock frequency, data transfer speed, bandwidth, data frame format, data rate, handshaking protocol, error detection, impedances, and line termination.

Parallel and Serial Buses

- A parallel bus carries data bits simultaneously, and a serial bus carries data bits sequentially one at a time.
- Figure 2 is a simple comparison of parallel and serial buses showing eight bits being transmitted.
- It seems that a **parallel bus** would transmit data faster than a serial bus because multiple data bits can be sent simultaneously. However, this is not always the case.
- As data rates increase, problems like crosstalk across parallel bus lines, timing skew between bus lines, and EMI (electromagnetic interference) limits the speed.
- **Serial buses** are not limited by those factors and can transmit data at higher rates than parallel buses in many situations.



(a) Parallel bus



(b) Serial bus

FIGURE 2 Comparison of parallel and serial buses

Internal and External Buses

☐ **Internal buses** carry information within a system, that is, from one part of the system to another part of the same system.

☐ **External buses** (also known as expansion buses) are used to connect one system to another separate system.

☐ **For example**, a computer connects to peripheral units such as a monitor, keyboard, mouse, and printer through external buses, as illustrated in Figure 3.

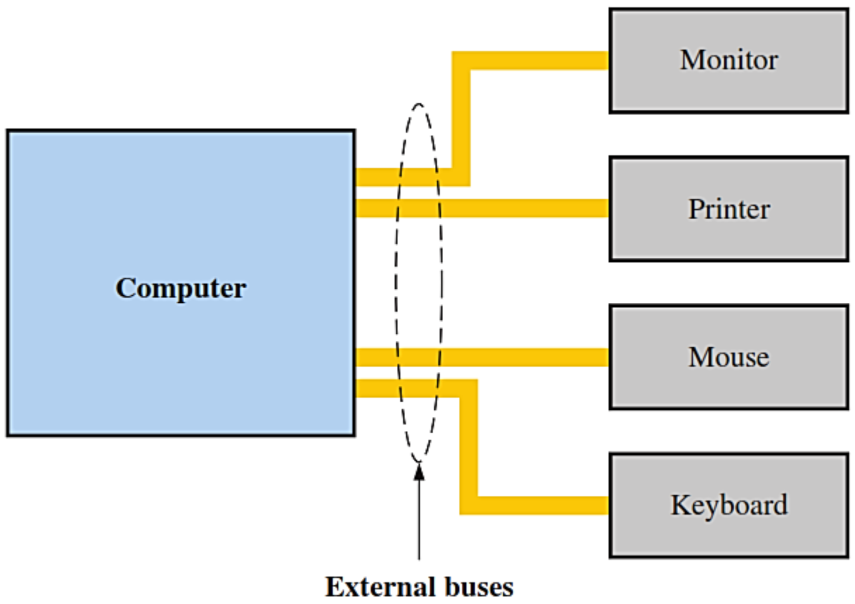


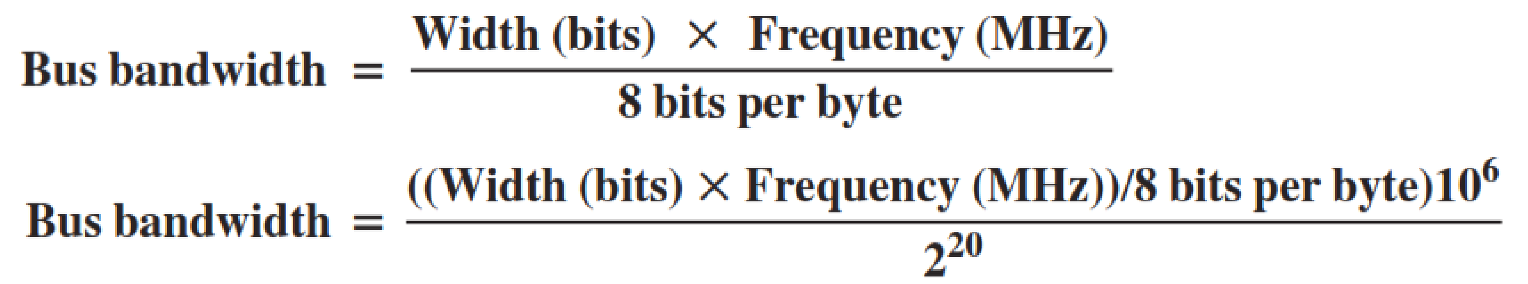
FIGURE 3 Example of external bus application

General Bus Characteristics

- A bus is typically described by the following parameters:
  - **Width:** The number of bits that a bus can transmit at one time. The width of typical buses can vary from 1 bit for a serial bus up to 64 bits for a parallel bus.
  - **Frequency:** The clock frequency at which a bus can operate.
  - **Transfer speed:** The number of bytes per clock cycle.
  - **Bandwidth:** The number of bytes per clock cycle times the number of clock cycles per second; that is, transfer speed times frequency. Bus bandwidth is sometimes called throughput.
- Bus bandwidth can be specified in two ways, which result in slightly different values. The difference depends on how the prefix M in MBps is defined.
- It can be defined in decimal form as a power of ten $(10^6 = 100{,}000)$ or in binary form as a power of two $(2^{20} = 1{,}048{,}576)$.

General Bus Characteristics

- In the decimal form, the M stands for mega; in the binary form, the M stands for mebi (mega-binary).
- The following two formulas provide for determination of the bus bandwidth.
- Equation 1 is for the decimal approach, and Equation 2 is for the binary approach.



$$\text{Bus bandwidth} = \frac{\text{Width (bits)} \times \text{Frequency (MHz)}}{\text{8 bits per byte}} \quad (1)$$

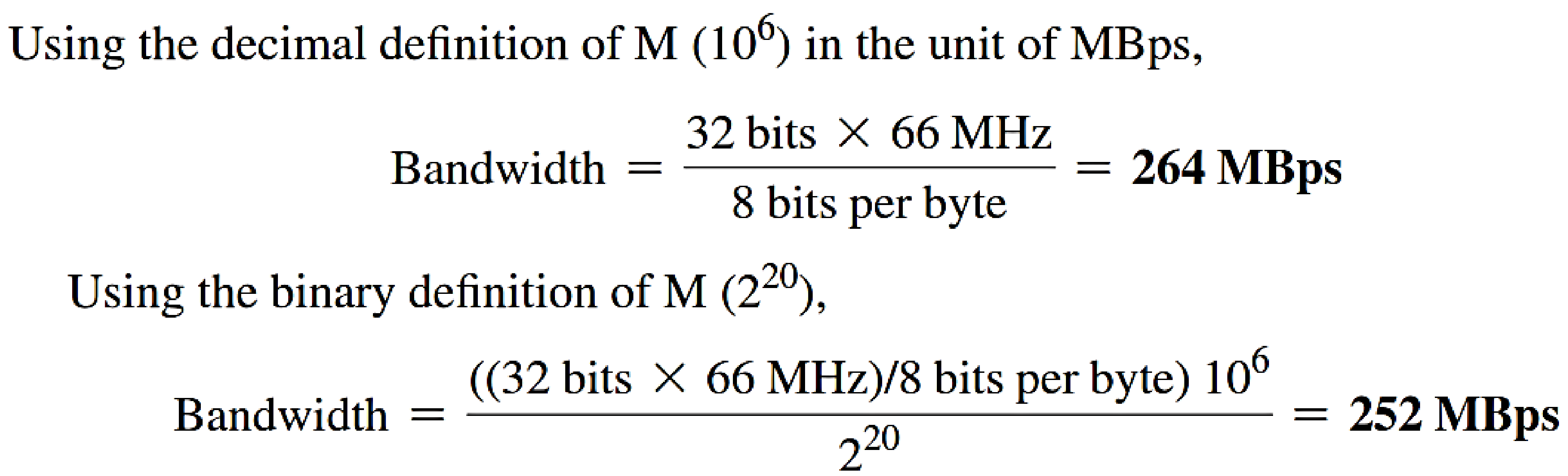
$$\text{Bus bandwidth} = \frac{((\text{Width (bits)} \times \text{Frequency (MHz)})/\text{8 bits per byte})10^6}{2^{20}} \quad (2)$$

General Bus Characteristics

EXAMPLE 1:

A certain bus is specified with a width of 32 bits and a frequency of 66MHz. Determine the bus bandwidth expressed as two different values, according to the decimal and binary definitions of M. Note that Bps is the bytes per second.

SOLUTION:



Using the decimal definition of M (10^6) in the unit of MBps,

$$\text{Bandwidth} = \frac{32 \text{ bits} \times 66 \text{ MHz}}{8 \text{ bits per byte}} = \mathbf{264\ MBps}$$

Using the binary definition of M (2^{20}),

$$\text{Bandwidth} = \frac{((32 \text{ bits} \times 66 \text{ MHz})/8 \text{ bits per byte})\ 10^6}{2^{20}} = \mathbf{252\ MBps}$$

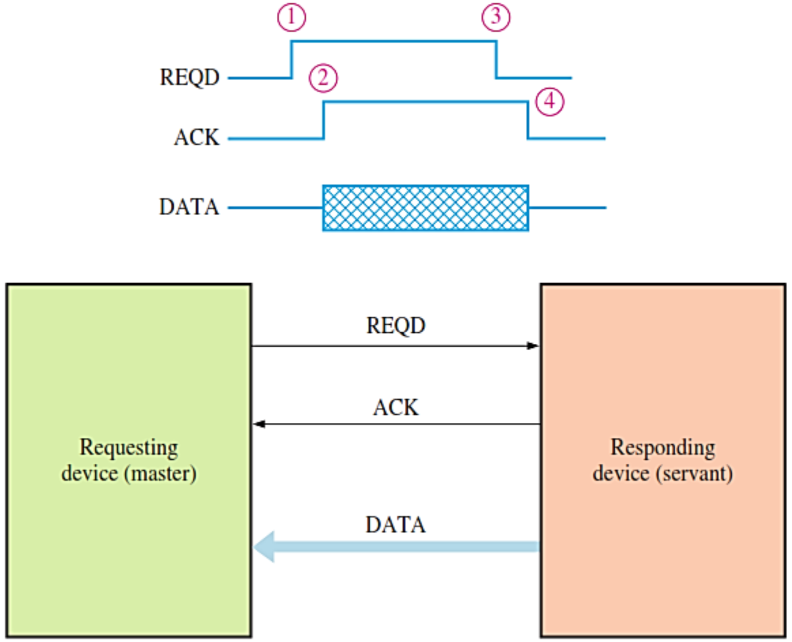
Bus Protocol

- Bus protocol is a set of rules that allow two or more devices to communicate through a bus.
- Buses provide for data transfer, address selection, and control.
- Each device connected to a bus has an address assigned to it for identification and command signals as well as control signals to implement the protocol.
- These signals allow the devices to work properly together by identifying each other and communicating back and forth.
- One device can send a request to another device and get an acknowledgement or reply per second.

Bus Protocol

Handshaking

- ☐ The handshake is a routine by which two devices initiate and complete a bus transfer.
- ☐ Figure 4 shows a simple handshake process, including a timing diagram, in which a requesting device (sometimes called the *master*) and a responding device (sometimes called the *servant*) initiate and complete a data transfer.



① Master sends request for data (REQD) to servant.
② Servant sends an acknowledgement (ACK) and places data on bus.
③ Master receives data and removes request.
④ Servant removes acknowledge and is ready for next request.

FIGURE 4 Simple example of handshake and data transfer

Synchronous and Asynchronous Buses

- A synchronized bus includes a clock in the control lines and has a fixed protocol that is relative to the clock.
- A synchronous bus is fast but has the disadvantage that every device connected to it must operate at the same clock frequency.
- Also, the physical length of the bus may be limited because of having to carry a high-frequency clock signal.
- An asynchronous bus is not clocked, so it can serve various devices with different clock rates.
- The asynchronous bus uses a handshake protocol to establish communication, as previously described.

Single-Ended vs. Differential Buses

- Data communications between devices can be classified as either single-ended or differential in terms of the physical bus configuration.
- In general, single-ended operation is limited in both data rate and distance (cable length). Differential operation provides much higher data rates and longer transmission distances.
- **Single-ended operation** uses one wire for data and one wire for ground, where the signal voltage on the wire is with respect to ground.
- **Differential operation** uses two wires for data and one wire for ground. The data signal is sent on one wire in the twisted pair and its complement (inversion) is sent on the other wire.
- The difference between the two data wires is the differential signal. Figure 5 shows both single-ended and differential operation.

Single-Ended vs. Differential Buses

- ☐ A single-ended transmission is simpler and lower in cost compared to a differential transmission.
- ☐ Differential operation is much less sensitive to noise because of rejection. This means that when a common noise signal appears on each line, the two noise signals cancel due to the differential operation where the difference between them is zero.
- ☐ Since the data signals are the same but opposite in phase, they are effectively added, and the data signal is reinforced while the noise signal is cancelled.
- ☐ Due to the twisted pair, crosstalk is reduced at higher frequencies, thus allowing longer cables.

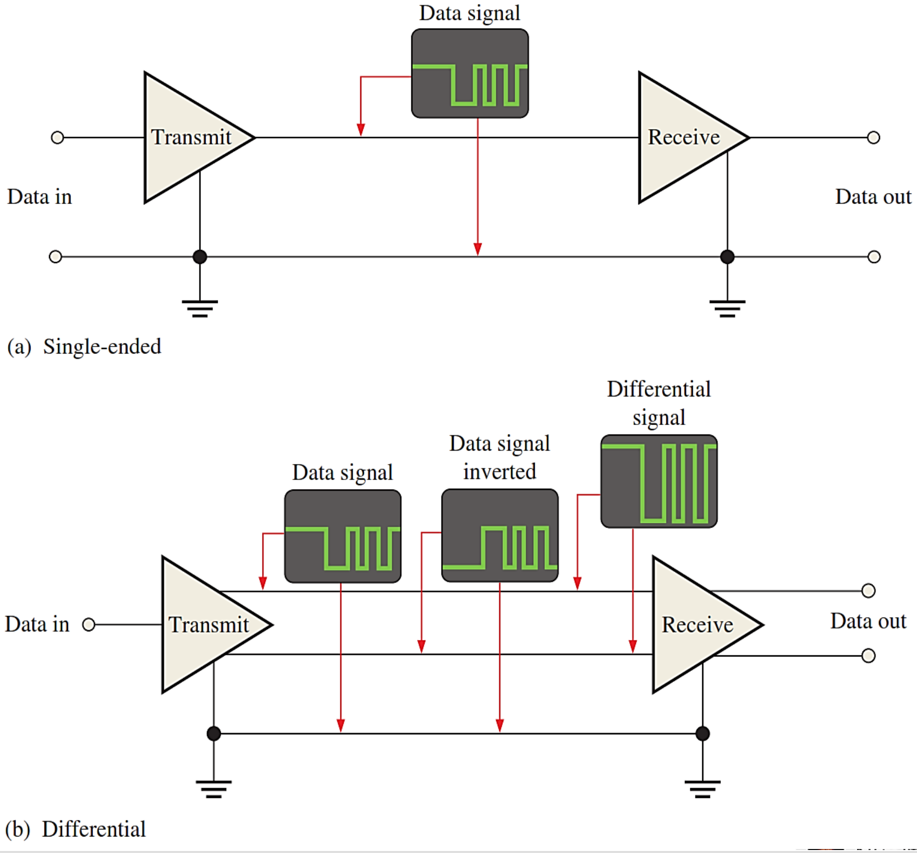


FIGURE 5 A comparison of single-ended and differential bus operation.

Parallel Buses: The PCI Bus

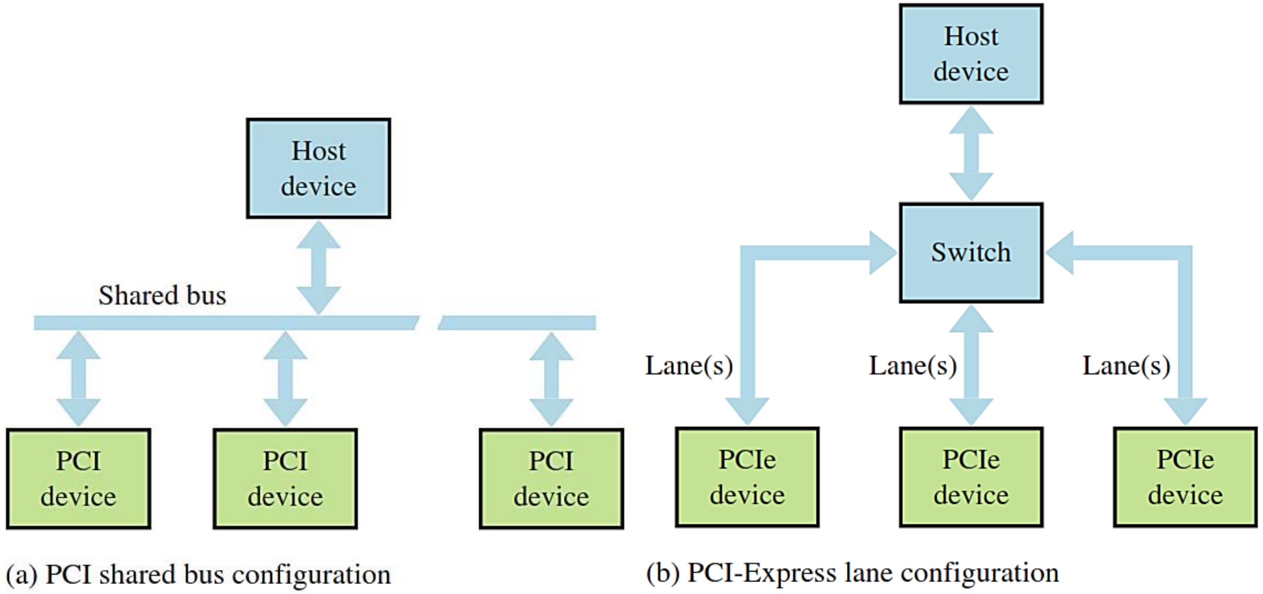
- ☐ The **PCI (peripheral component interconnect)** bus is an internal synchronous bus for inter-connecting chips, expansion boards, and processor/memory subsystems.
- ☐ The original PCI bus had a width of 32 bits and a frequency of 33 MHz. Another version has a width of 64 bits and a frequency of 66 MHz. Still later versions enable 64-bit data transfers using up to a 133 MHz clock to enable bandwidths of up to 1066 MBps.
- ☐ The original PCI standard required 5 V power and signal levels. As the standard evolved, the option for 3.3 V was added. The latest standard provides for 3.3 V only.
- ☐ The **32-bit** PCI connector has 62 pins and 124 contacts (62 per side). Thirty-two of the contacts are used for both a 32-address and 32 bits of data, which are multiplexed. The remaining pins are used for command and control signals, power, ground, etc.
- ☐ A **64-bit** PCI connector has an additional 32 pins for a total of 94.

Parallel Buses: The PCI-X Bus

- The **PCI-X bus** is a high-performance enhancement of the PCI and is backward compatible with the PCI bus,
- Although it is a faster bus and has some additional features.
- A 64-bit bus ,the PCI-X runs at a frequency of 133 MHz.
- The PCI-X 2.0 revision supports frequencies of 266 MHz and 533 MHz.
- Some additional features increase system reliability by minimizing errors at high transfer rates.
- Servers are the major application for PCI-X.

Parallel Buses: The PCI-Express Bus

- ☐ The **PCI-Express** is also designated as PCIe or PCI-E. This bus differs from the PCI and PCI-X buses in that it does not use a **shared bus**.
- ☐ Both PCI and PCI-X use a shared bus configuration, as shown in Figure 6(a). Each PCIe device has a dedicated path, called a *lane*, to a single chip known as a *switch*, as shown in part (b).
- ☐ More lanes result in a faster data transfer. High speed makes PCI-Express ideal for video and grap.
- ☐ A single PCI-Express lane contains two pairs of conductors. One pair of conductors from a given device receives data and the other pair sends data in a serial format.



(a) PCI shared bus configuration

(b) PCI-Express lane configuration

FIGURE 6 Comparison of PCI and PCI-Express

Parallel Buses: The PCI-Express Bus

- ☐ A single lane configuration is known as x1 and is illustrated in Figure 7(a). A x2 configuration is shown in part (b), and a x16 configuration is shown in part (c). Other possible configurations are x4, x8, and x32.
- ☐ Bidirectional data are transferred serially on each lane. For multiple-lane configurations, the serial data on each lane are in parallel with the serial data on all the other lanes. The data are transferred at one bit per cycle on a x1 connection, two bits per cycle on a x2, and sixteen bits per cycle on a x16.
- ☐ The PCI-Express has a bandwidth of 4 Gbps per lane. PCI-Express supports *hot swapping* in which expansion cards can be added or removed without turning off the system. PCI and PCIe are software compatible but not hardware compatible.

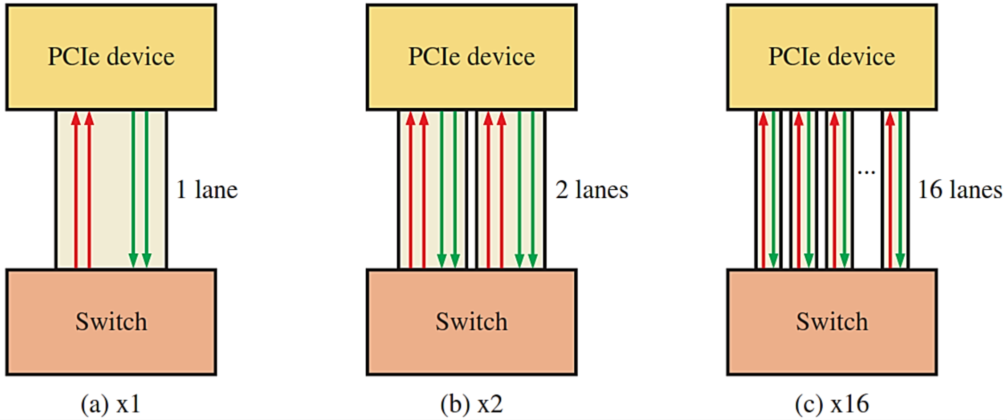


FIGURE 7 PCI-Express lane configurations

Parallel Buses: The IEEE-488 Bus

- This bus standard has been around a long time and is also known as the **General-Purpose Interface Bus (GPIB)**. Widely used in test and measurement applications, it was developed by Hewlett-Packard in the 1960s.
- The IEEE 488 specifies 24 lines that are used to transfer eight parallel data bits at a time and provide eight control signals that include three handshake lines and five bus-management lines.
- Also included are eight ground lines used for shielding and ground returns. The maximum data transfer rate for the IEEE 488 standard is 1 Mbps. A superset of this standard, called the HS488, has a maximum data rate of 8 Mbps.
- To connect test equipment to a computer using the IEEE-488 bus, an interface card is installed in the computer, which turns the computer into a system controller.

Parallel Buses: The IEEE-488 Bus

- In a typical GPIB setup, up to 14 controlled devices (test and measurement instruments) can be connected to the system controller.
- When the system controller issues a command for a controlled device to perform a specified operation, such as a frequency measurement, it is said that the controller "**talks**" and the controlled device "**listens**."
- A **listener** is an instrument capable of receiving data over the GPIB when it is addressed by the stem controller (computer). Examples of listeners are printers, monitors, programmable power supplies, and programmable signal generators.
- A talker is an instrument capable of sending data over the GPIB. Examples are DMMs and frequency counters that can output bus-compatible data.
- Some instruments can send and receive data and are called talker/listeners; examples are computers, modems, and certain measurement instruments.

Parallel Buses: The IEEE-488 Bus

- ☐ The system controller can specify each of the other instruments on the bus as either a talker or a listener for the purpose of data transfer. The controller is usually a talker/listener.
- ☐ A typical GPIB arrangement is shown in Figure 8 as an example.
- ☐ The three **basic bus signal** groupings are shown as the *data bus, data transfer control bus, and interface management bus.*

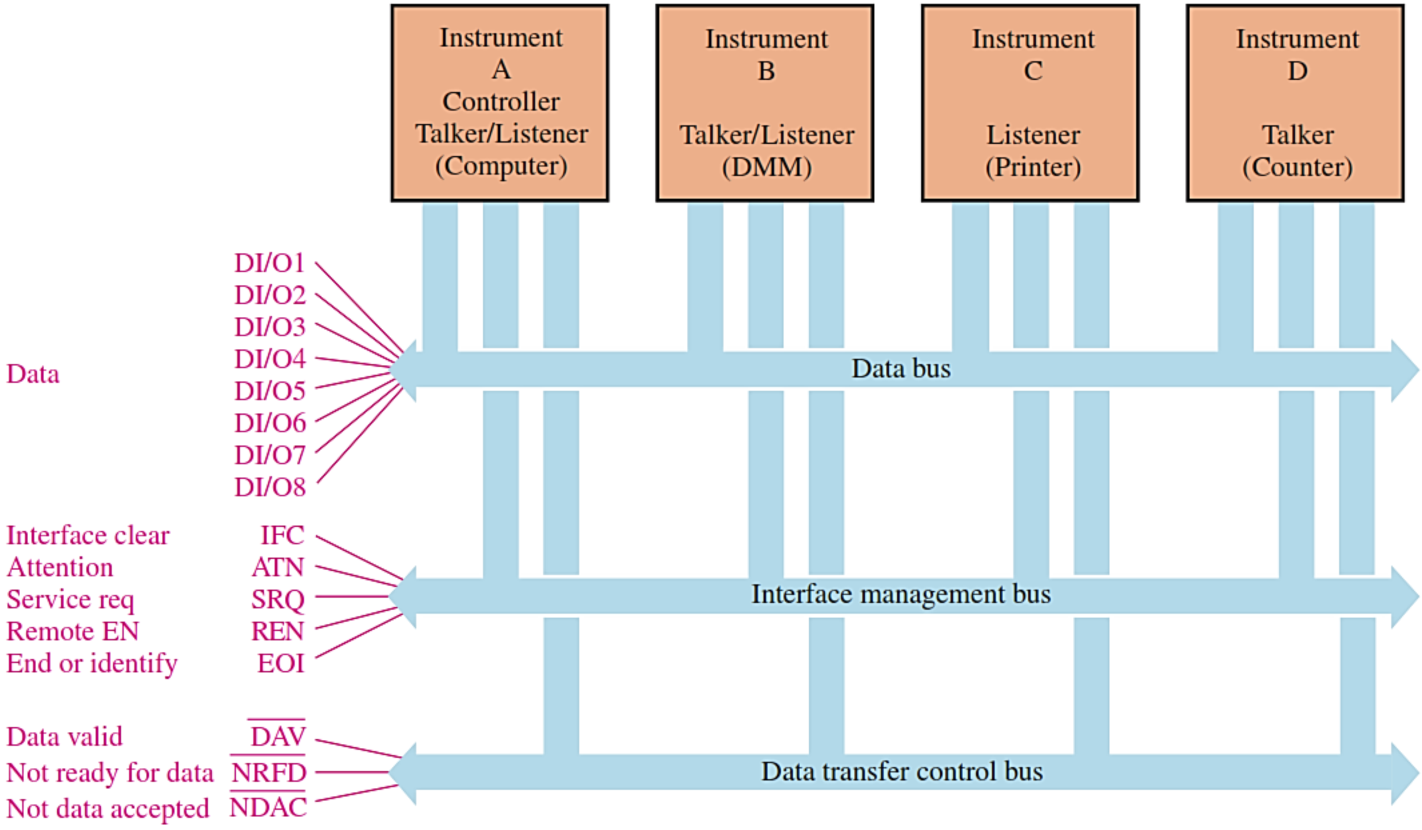


FIGURE 8 A typical IEEE 488 (GPIB) connection.

Parallel Buses: The IEEE-488 Bus

- ☐ The parallel data lines are designated DI/O1 through DI/O8 (data input/output). One byte of data is transferred on this bidirectional part of the bus.
- ☐ Every byte that is transferred undergoes a handshaking operation via the data transfer control.
- ☐ The three active-LOW handshaking lines indicate if data are valid (DAV), if the addressed instrument is not ready for data (NRFD), or if the data are not accepted (NDAC).
- ☐ More than one instrument can accept data at the same time, and the slowest instrument sets the rate of transfer. Figure 9 shows the timing diagram for the GPIB handshaking sequence, and Table 2 describes the handshaking signals.

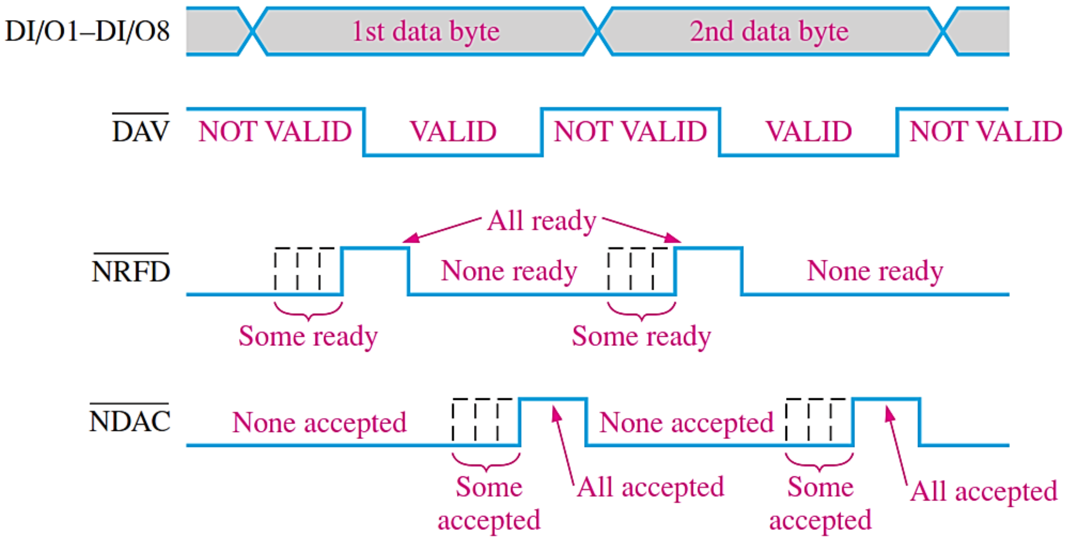
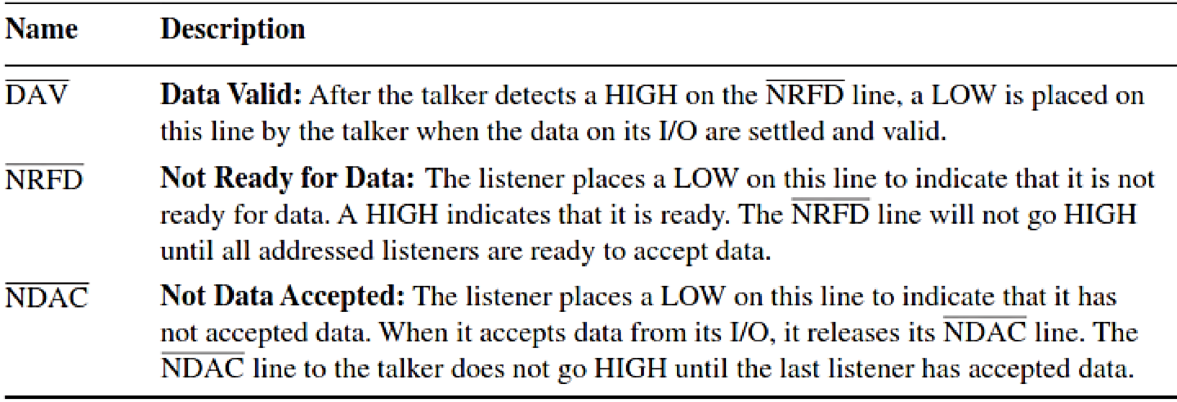


FIGURE 9 Timing diagram for the GPIB handshaking sequence

Parallel Buses: The IEEE-488 Bus

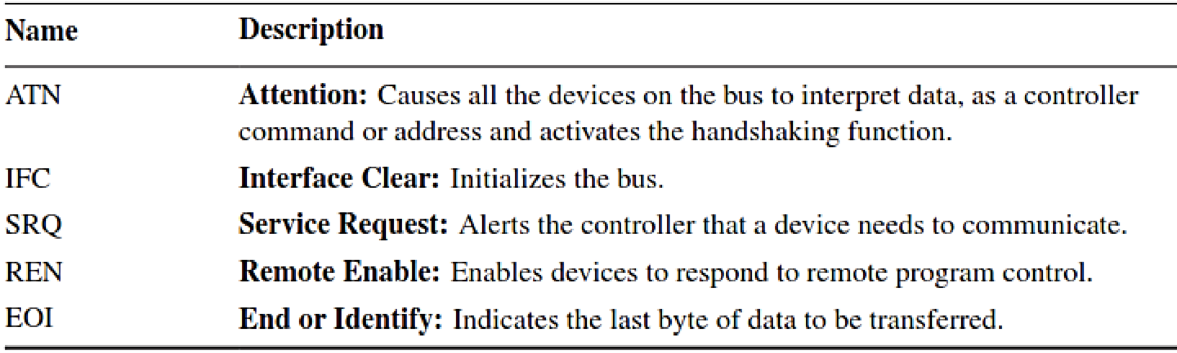
- The **five signals** of the interface management bus control the orderly flow of data. The ATN (attention) line is monitored by all instruments on the bus.
- When ATN is active, the system controller selects the specific interface operation, designates the talkers and the listeners, and provides specific addressing for the listeners.
- Each GPIB instrument has a specific identifying address that is used by the system controller. Table 3 describes the GPIB interface management lines and their functions.

TABLE 2 The GPIB handshaking signals.



Name	Description
$\overline{\text{DAV}}$	**Data Valid:** After the talker detects a HIGH on the $\overline{\text{NRFD}}$ line, a LOW is placed on this line by the talker when the data on its I/O are settled and valid.
$\overline{\text{NRFD}}$	**Not Ready for Data:** The listener places a LOW on this line to indicate that it is not ready for data. A HIGH indicates that it is ready. The $\overline{\text{NRFD}}$ line will not go HIGH until all addressed listeners are ready to accept data.
$\overline{\text{NDAC}}$	**Not Data Accepted:** The listener places a LOW on this line to indicate that it has not accepted data. When it accepts data from its I/O, it releases its $\overline{\text{NDAC}}$ line. The $\overline{\text{NDAC}}$ line to the talker does not go HIGH until the last listener has accepted data.

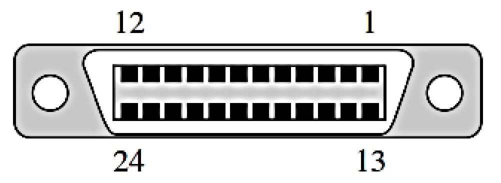
TABLE 3 The GPIB management lines.

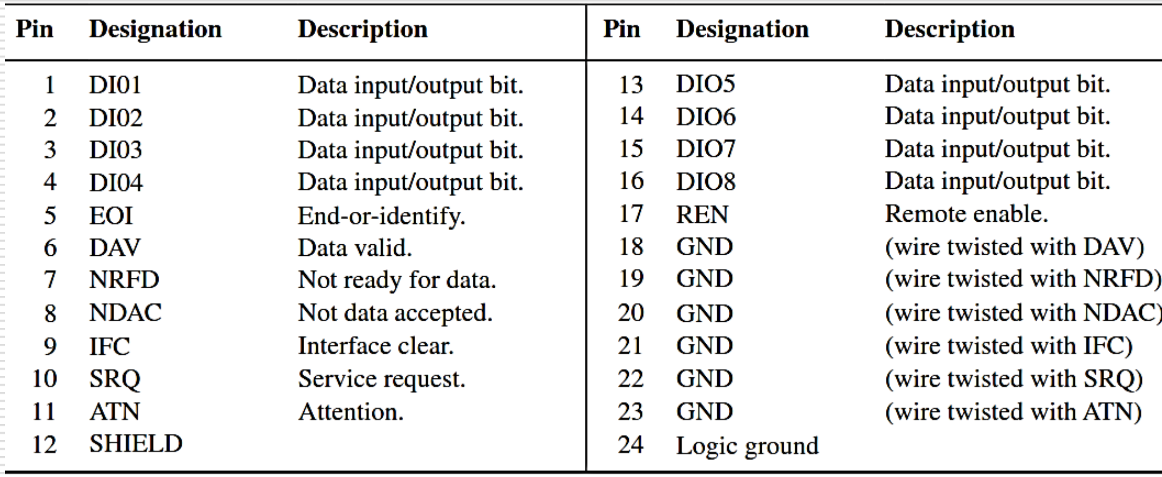


Name	Description
ATN	**Attention:** Causes all the devices on the bus to interpret data, as a controller command or address and activates the handshaking function.
IFC	**Interface Clear:** Initializes the bus.
SRQ	**Service Request:** Alerts the controller that a device needs to communicate.
REN	**Remote Enable:** Enables devices to respond to remote program control.
EOI	**End or Identify:** Indicates the last byte of data to be transferred.

Parallel Buses: The IEEE-488 Bus

- ☐ The GPIB is limited to a maximum cable length of 15 meters, and there can be no more than one instrument per meter with a maximum capacitive loading of 50 pF each.
- ☐ The cable length limitation can be overcome by the use of bus extenders and modems.
- ☐ A bus extender provides for cable-interfacing of instruments that are separated by a distance greater than allowed by the GPIB specifications or for communicating over greater distances via modem-interfaced telephone lines.
- ☐ The IEEE-488 connector and pin configuration are shown in Figure 10.





Pin	Designation	Description	Pin	Designation	Description
1	DI01	Data input/output bit.	13	DIO5	Data input/output bit.
2	DI02	Data input/output bit.	14	DIO6	Data input/output bit.
3	DI03	Data input/output bit.	15	DIO7	Data input/output bit.
4	DI04	Data input/output bit.	16	DIO8	Data input/output bit.
5	EOI	End-or-identify.	17	REN	Remote enable.
6	DAV	Data valid.	18	GND	(wire twisted with DAV)
7	NRFD	Not ready for data.	19	GND	(wire twisted with NRFD)
8	NDAC	Not data accepted.	20	GND	(wire twisted with NDAC
9	IFC	Interface clear.	21	GND	(wire twisted with IFC)
10	SRQ	Service request.	22	GND	(wire twisted with SRQ)
11	ATN	Attention.	23	GND	(wire twisted with ATN)
12	SHIELD		24	Logic ground	

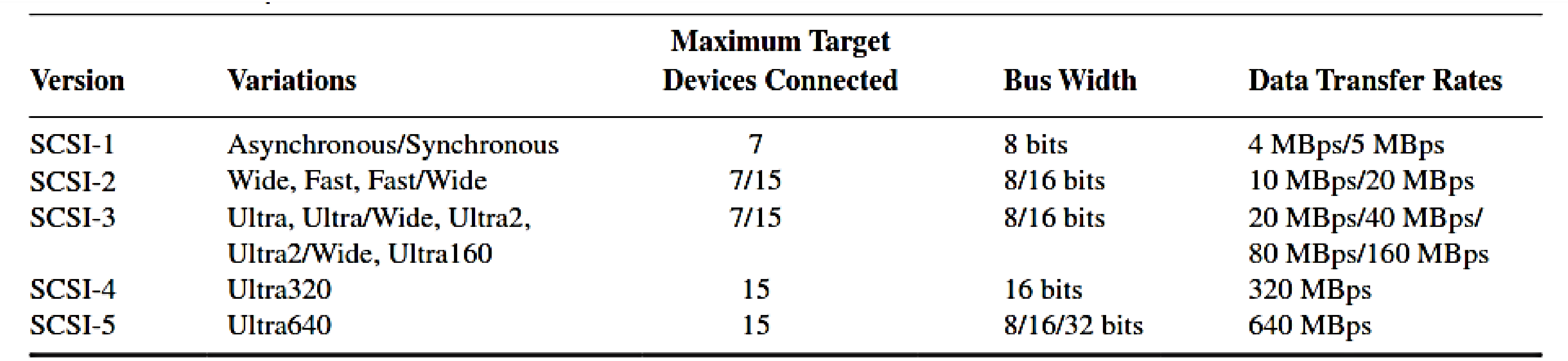
FIGURE 10 The IEEE-488 (GPIB) bus connector and pin assignments

Parallel Buses: The Parallel SCSI Bus

- The **SCSI (small computer system interface) bus**, generally pronounced “skuzy”, is a parallel I/O bus with a width of either 8, 16, or 32 bits, depending on the version.
- For many years SCSI has been one of the most widely used buses in storage servers and data centers. SCSI is also used for the purpose of transferring data between a computer and peripheral devices, such as hard disks, tape drives, scanners, and CD drives.
- The original version of the SCSI parallel bus standard was introduced in 1986 and designated SCSI-1.
- The current SCSI standard is known as SCSI-5, which was preceded by SCSI-1, SCSI-2, SCSI-3, and SCSI-4. Later versions are backward compatible with earlier versions.
- There are many variations of the SCSI standard version with designations such as asynchronous, synchronous, fast, ultra, and wide, which have different speeds, widths, and number of devices that can be connected, as shown in Table 4.

Parallel Buses: The Parallel SCSI Bus

TABLE 4 Evolution of the parallel SCSI standard



Version	Variations	Maximum Target Devices Connected	Bus Width	Data Transfer Rates
SCSI-1	Asynchronous/Synchronous	7	8 bits	4 MBps/5 MBps
SCSI-2	Wide, Fast, Fast/Wide	7/15	8/16 bits	10 MBps/20 MBps
SCSI-3	Ultra, Ultra/Wide, Ultra2, Ultra2/Wide, Ultra160	7/15	8/16 bits	20 MBps/40 MBps/ 80 MBps/160 MBps
SCSI-4	Ultra320	15	16 bits	320 MBps
SCSI-5	Ultra640	15	8/16/32 bits	640 MBps

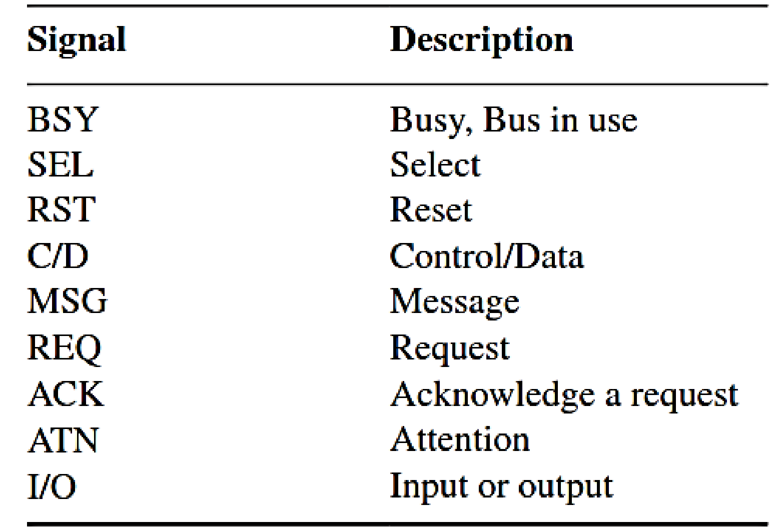
- ☐ A parallel SCSI bus contains nine control signals in addition to data, dc voltages, and ground. These signals are listed in Table 5.

Parallel Buses: The Parallel SCSI Bus

SCSI Signals

- Up to eight or sixteen devices, including the host, can be connected to a SCSI bus, but only two devices can communicate at any given time.
- Communication begins when an initiating device sends a request, and the target device acknowledges and performs the request.
- Single-ended (SE) and differential (LVD or HVD) are the three electrical specifications. Single-ended operation is limited to a cable length of 6 meters, and differential operation allows up to 25 meters.
- LVD is low-voltage differential and HVD is high-voltage differential. SCSI devices can operate either asynchronously or synchronously.

TABLE 5: SCSI parallel bus signals



Signal	Description
BSY	Busy, Bus in use
SEL	Select
RST	Reset
C/D	Control/Data
MSG	Message
REQ	Request
ACK	Acknowledge a request
ATN	Attention
I/O	Input or output

END of Lecture # 06